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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,878	06/28/2001	Jun Dong Kim	08245.0027	3043

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EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,878	KIM ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

Applicants' request for reconsideration filed on September 19, 2002 has been entered on September 25, 2002.

Therefore claims 1-10 as originally filed are currently pending in the application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The previous rejection based on the phrase " material layer" in claim 6 that renders it indefinite is maintained and made Final.

Applicants' contention that their disclosure includes exemplary embodiments that render the term " material layer " clear is not persuasive because the Examiner could not locate in the specification as originally filed the exemplary embodiments that render the term " material layer " clear. The Examiner's search located a single mention of layer 22 in page 5 of the specification wherein (i.e. page 5) it does not specify what constitutes the material layer .

Applicants' argument that Examiner's line of reasoning (" applicants' disagree with the Examiner's position that the phrase " material layer" may further the specification and that one skilled in the art would be unable to determine what is defined by the phrase") would unnecessarily restrict Applicants' in the use of different terms,

phrases and/or expressions when claiming an invention is not persuasive because the issue is whatever terms phrases and /or expressions used in claiming applicants' invention is sufficiently described with enough clarity that one skilled in the art would be able to follow it and not whether an applicant can or cannot use different terms, phrases and /or expressions.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ye et al. (U.S. Patent No. 6,080,529 herein after Ye) in view of Lau et al. (U.S. Patent No. 5,173,542, herein after Lau) for reasons previously set out and reproduced below for ready reference. For response to Applicants' arguments see " response to arguments section" below.

With respect to claim 1, Ye describes a method of forming gate electrodes of a semiconductor device including the steps of : forming a gate insulation layer over the semiconductor wafer (Ye col. 11 lines 36-38, silicon dioxide layer not shown in the drawings), forming a conductive layer over the gate insulation layer (Ye fig. 2a # 216, col. 11 line 41), forming a low-dielectric layer over the conductive layer (Ye fig. 2A # 218, col. 11 line 42), forming a photo resist pattern whose width is equal to the exposure limit on the low dielectric layer (Ye layer 224 or 324, col. 21 lines 55-65, col. 22 lines 1-2 , col. 6 lines 5-21, especially line 18), patterning the low dielectric layer using the

photo resist pattern as a mask (Fig. 2c , col. 6 lines 9- 18, col. 12 lines 28-32), removing photo resist pattern (col.11 lines 33-34), shrinking the low dielectric pattern.

Ye does not specifically mention shrinking the low dielectric pattern.

However, Lau, a patent from the same filed of endeavor (both Ye and Lau deal low dielectric layers made from organic polymers Including PTFE, etc. see claim 3 of Ye and col. 1 lines 20-37 of Lau) describes the standard procedure of the shrinking the low-dielectric pattern by curing the low-dielectric pattern (Lau in col.14 line 37 and claim 11 © curing) to cross link the polymers.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Lau's curing (i.e. shrinking of dielectric) step in Ye's method steps to cross-link the polymer of the low dielectric layer . (Lau col. 1 lines 49-61).

Forming gate electrodes by patterning the conductive layer and the gate insulation layer using the shrunken low dielectric layer pattern as a mask (Figs. 3D and 2 B, col. 11 lines 66- col. 12 lines 32, col. 15 lines 6-10). (it is noted that Ye teaches at least two separate embodiments in figs. 2A—G and 3 A-G, however Ye in at least col. 15 lines 5-8 teaches the steps of embodiments in figs. 2 and 3 are interchangeably used).

With respect to claim 2 wherein the low-dielectric layer is formed of an organic spin-on glass or inorganic spin-on glass layer. (Ye col. 6 lines 22-26-organic low k dielectric materials and col. 14 line 65-66 glass-like siloxane) .

With respect to claim 3 wherein the forming of the low –dielectric layer comprises : depositing low dielectric layer over the conductive layer for the gate electrodes (fig.2

G # 230, col. 13 lines 55-60) and soft –baking the low-dielectric layer at a predetermined temperature .

Ye does not specifically describe soft-baking its low-dielectric layer at a predetermined temperature.

However, Lau, a patent from the same filed of endeavor describes in col. 14 line 35 the standard procedure of soft –baking the low dielectric is soft baked after its application to drive off any remaining solvents from the mixture applied.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Lau standard " soft-baking step in Ye's method to remove any excess liquid remaining after the application of the dielectric polymer mixture on the wafer. (Lau col.14 Line 36).

With respect to claim 4, wherein the shrinking the low-dielectric pattern by curing the low-dielectric pattern at 400-500 degrees centigrade. (Lau in col.14 line 37 and claim 11 © curing at 300-450 degrees to cross link the polymers). Therefore it would have been obvious to curing between 400-500 degrees without more because it was previously done in the over lapping range of 300-450 degrees.

With respect to claim 5, wherein removing the photo resist pattern and shrinking are performed at the same time. (Ye in col. 4 lines 21-29 and col. 11 lines 1-7describes the process of removing the photo resist pattern using temperature between 150-350 degrees centigrade which temperature falls within the standard soft-temperature of 100-200 (Lau col. 14 line 36) therefore Ye's step of removing the photo resist will also result in the sift bake of the wafer).

With respect to claim 6, to the extent understood, it recites the same steps as claim 1 except for reciting, " a material layer" instead of a "conductive layer " in claim 1 and rejected for the same reasons as stated above under claim 1 . (It is noted that the sequence of performing the process steps is slightly changed in claim 6, however as well settled case law (Exparte Rubin and In re Burhaus , any order of performing steps is prima facie obvious in absence of new or unexpected results).

Claims 7-10 repeat the same steps of claims 2-5 and are rejected for reasons stated above.

Response to Arguments

Applicant's arguments filed September 19, 2002 have been fully considered but they are not persuasive for the following reasons.

It is noted that Applicants' arguments are based on piece meal attacks on references, it has been held that one cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combinations of references. In re Keller, 208 USPQ 871 (CCPA 1981).

Applicants' first contention is that Ye does not teach or suggest the relationship between the width of the photoresist pattern based on an exposure limit of layer supporting the pattern is not persuasive because Ye (as previously stated in col. 21 lines 55-65, col. 22 lines 1-2, col. 6 lines 5-21 , col. 1 lines 32-37, col. 5 lines 48-53) teaches a lower aspect ratio in high temperature pattern-imaging methods that include an etching process which permits the development of patterning masks which can transfer a desired pattern to adjacent layers in a manner which reduces or avoids the

formation of mask residue on the etched structure and further states devices with 0.25um or smaller can be made with precise profile and avoidance of residue.

All of the above clearly show that the aspect ratio (which is different from the masking layer thickness) includes the relationship between the width of the photoresist pattern and the exposure limit (for a given dimension of the device) of the layer supporting the pattern and further shows forming patterns without mask residue, in other words even exposing the upper layer to its maximum possible limit (including its width) produces a pattern on the underlying layer without any mask residue i.e. shows exposure up to the width limit . Thus Ye teaches the relationship between the width of the photoresist pattern based on an exposure limit of layer supporting the pattern.

Applicants' next contention that Lau does not teach or suggest shrinking a low dielectric pattern that is formed on a multi layered semiconductor device is also not persuasive because Applicants' are again trying to show non obviousness by attacking references individually it has been held that one cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combinations of references. In re Keller, 208 USPQ 871 (CCPA 1981).

It is noted that the rejection was based on the combined teachings of Ye (showing a multi layered semiconductor device) and Lau (shrinking a low dielectric pattern) and applicants' present argument does not provide any reason why the combined teachings do not render the claims obvious.

The motivation to combine the references was previously provided and reproduced above and restated here again, as Lau specifically describes its polymers

as being used for insulation, coating, films and interlayer insulating material in multi layer electronic circuit (Lau col.1 lines 14-20, 37-39, etc.) one of ordinary skill in the art would be motivated to combine the teachings of Lau and Ye. i..e. Ye and Lau both are from the same filed of endeavor, namely processing interlayer insulating material in multilayer electronic circuits, and the motivation to combine Ye and Lau include Lau's curing (i.e. shrinking of dielectric) step in Ye's method steps to cross-link the polymer of the low dielectric layer (Lau col. 1 lines 49-61) by a method wherein the steps/ ingredients are conveniently controllable with stable cross linking sites and do not introduce undesirable functionalities into the polymeric composition being cross linked.

Claim 6 was alleged to be allowable for the same reasons stated under claim 1, however as shown above the reasons are not persuasive and therefore claim 6 is also not allowable.

Dependent claims 2-5 and 7-10 were alleged to be allowable as they depend from allegedly allowable claims 1 and 6.

However as shown claims 1 and 6 are not allowable and therefore claims 2-5 and 7-10 are also not allowable.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

As the same references as previously applied are also used here this forms a separate basis for making this action Final.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

SR

Steven H. Rao

Patent Examiner

November 27, 2002

SUPERVISORY
TECHNOLOGY CEN